What is claimed is:

1. A connection package for connecting at least one high speed integrated circuit chip ("IC") to external terminals, said IC having a plurality of signal pads, said connection package comprising:

a substrate;

a plurality of microstrips on said substrate,

said plurality of microstrips for providing transmission between said plurality of signal pads and said external terminals,

at least a pair of said plurality of microstrips for transmitting signals from or to said IC,

said pair of said plurality of microstrips ("said pair of microstrips") for being capacitively coupled to each other, through a first partial length,

said pair of microstrips for having substantially constant characteristic impedance throughout substantially the entire length of said pair of microstrips.

2. The connection package of claim 1, wherein said pair of microstrips has a width that increases as it is outwardly routed.

3. The connection package of claim 1, wherein a width of each of said pair of microstrips along said first partial length is less than a width determined from an equation 50 ohm = 1 / vC, where v is a velocity of propagation of the signals and C is a capacitance per unit length.

4. The connection package of claim 1, wherein said substrate is made of substantially Alumina.

5. The connection package of claim 1, wherein said IC is a demultiplexor or multiplexor chip for OC-768 applications.

6. The connection package of claim 1, wherein said signals comprise high-speed data signals operating at a frequency of at least 20 Gbps.

7. The connection package of claim 1, wherein said external terminals comprise a

pair of coaxial terminals.

8. The connection package of claim 1, wherein said first partial length is located substantially at a first end of said pair of microstrips,

wherein said first end is located near an inner edge of said substrate for receiving said signals from said IC.

9. The connection package of claim 1, wherein a second partial length within said first partial length of said pair of microstrips is widened to increase its capacitance.

10. The connection package of claim 9, wherein said second partial length is located substantially at a first end of said pair of microstrips,

wherein said first end is located near an inner edge of said substrate for receiving said signals from said IC.

11. The connection package of claim 7, wherein a second partial length within said first partial length of said pair of microstrips is widened to increase its capacitance.

12. The connection package of claim 1, wherein a width of each of said pair of microstrips along a portion of said first partial length is not more than 5 mils,

wherein spacing between said pair of microstrips along a portion of said first partial length is not more than 5 mils.

13. The connection package of claim 1, wherein said pair of microstrips is substantially 50-ohm transmission lines throughout substantially the entire length of said pair of microstrips.

14. The connection package of claim 1, wherein said signals are differential signals.

15. The connection package of claim 1, wherein said substrate is a single-layer substrate.

16. The connection package of claim 1, wherein said substrate is a multiple-layer substrate.

17. The connection package of claim 7, wherein a width of a dielectric ring portion of one of said pair of coaxial terminals is substantially identical to a thickness of said substrate.

18. The connection package of claim 1, wherein said external terminals comprise

GPPO connectors.

19. The connection package of claim 7, wherein a width of a dielectric ring portion of one of said pair of coaxial terminals is substantially identical to a thickness of said substrate.

20. The connection package of claim 1, wherein said pair of microstrips are for transmitting high-speed signals,

wherein said plurality of microstrips further comprise a second plurality of microstrips that are for transmitting low speed signals.

**21.** A connection package for connecting at least one high speed integrated circuit chip ("IC") to external terminals, said IC having a plurality of signal pads, said connection package comprising:

(1) a substrate;

(2) means for providing transmission paths between said plurality of signal pads and said external terminals;

(3) means for providing a pair of microstrips on said substrate for transmitting signals from or to said IC,

(4) means for providing capacitive coupling between said pair of microstrips through a first partial length of said pair of microstrips;

(5) means for providing substantially constant characteristic impedance throughout substantially the entire length of said pair of microstrips.

22. The connection package of claim 21, wherein a second partial length within said first partial length of said pair of microstrips is widened to increase its capacitance.

**23.** A system comprising:

a first package comprising:

a first high speed integrated circuit chip ("IC"), said IC having a plurality of signal pads,

a substrate;

external terminals;

a plurality of microstrips on said substrate,

said plurality of microstrips coupled between said plurality of signal pads and said external terminals,

said plurality of microstrips for being capacitively coupled to each other, through a first partial length,

said plurality of microstrips positioned closer in proximity to each other at said first partial length,

said plurality of microstrips for having substantially constant characteristic impedance throughout substantially the length of said plurality of microstrips,

a second package comprising a second IC;

a printed circuit board comprising said first package and said second package.

24. The system of claim 23, wherein a second partial length within said first partial length of said plurality of microstrips is widened to increase its capacitance,

wherein said first partial length and said second partial length are located near said signal pads.

**25.** A connection package for connecting at least one high speed integrated circuit chip ("IC"), said IC comprising at least a first signal and a second signal, said first and second signals being differential signals, the connection package comprising:

a dielectric substrate plate having a recess at its substantial center for said IC to be positioned;

a plurality of external terminals at a perimeter of said dielectric substrate plate;

a first transmission strip formed on a top surface of said dielectric substrate plate, said first transmission strip for connecting said first signal to a first terminal of said plurality of external terminals;

a second transmission strip formed on said top surface of said dielectric substrate plate, said second transmission strip for connecting said second signal to a second terminal of said plurality of external terminals;

wherein both said first and second transmission strips have a first partial length positioned to be capacitively coupled to one another near said IC,

wherein both said first and second transmission strips are for having substantially constant characteristic impedance throughout substantially the length of said first and second transmission strips.

26. A connection package of claim 25, wherein said dielectric substrate plate is made of substantially Alumina.

27. A connection package of claim 25, wherein said plurality of external terminals comprise coaxial terminals for connecting to said first and second transmission strips.

28. A connection package of claim 25, wherein plurality of external terminals are Gilbert connectors.

29. A connection package of claim 25, wherein a second partial length of said first and second transmission strips within said first partial length is widened to achieve a predetermined capacitance.

**30.** A connection package for connecting at least one high speed integrated circuit chip ("IC"), said IC comprising at least a first signal and a second signal, said first and second signals being differential signals, the connection package comprising:

(1) a substrate having a recess for said IC to be positioned;

(2) means for providing external transmission to said IC;

(3) means for connecting said first signal to said (2) means, said (3) means formed on top of said substrate;

(4) means for connecting said second signal to said (2) means, said (4) means formed on top of said substrate;

(5) means for providing partial capacitive coupling between said (3) means and said (4) means near said recess;

(6) means for maintaining substantially constant characteristic impedance from said IC to said (3) means and said (4) means,

(7) means for minimizing capacitive coupling between said (3) means and said (4) means near said (2) means.

**31.** A connection package for connecting at least one high speed integrated circuit chip ("IC"), said IC comprising at least one high speed signal and low speed signals, said connection package comprising:

a substrate;

at least one external coaxial connector for communicating said high-speed signal,

an array of terminals at a bottom side of said substrate for communicating at least said low speed signals;

a plurality of first microstrips selectively formed on a top surface of said substrate,

at least one of said plurality of first microstrips being disposed for connecting said high speed signal between said IC and said at least one external coaxial connector,

at least another one of said plurality of first microstrips being disposed for connecting one of said low speed signals between said IC and said array of terminals;

a plurality of interconnections formed within said substrate,

wherein at least one of said plurality of interconnections connects at least said at least another one of said plurality of first microstrips to at least one terminal of said array of terminals,

wherein said at least one of said plurality of first microstrips and said at least one external coaxial connector are for providing substantially constant characteristic impedance throughout substantially said at least one of said plurality of first microstrips and said at least one external coaxial connector.

32. The connection package of claim 31, wherein a rate of said high speed signal is at least 20 Gbps, and a rate of one of said low speed signals is lower than 20 Gbps.

33. The connection package of claim 31, wherein said at least another one of said plurality of first microstrips is for providing substantially constant characteristic impedance,

wherein at least one of said plurality of interconnections is for providing substantially constant characteristic impedance throughout said at least one of said plurality of

interconnections connecting at least said at least another one of said plurality of first microstrips to at least one terminal of said array of terminals.

34. The connection package of claim 31, wherein said at least one external coaxial connector is placed on a side of said substrate.

35. The connection package of claim 31, said high-speed signal does not transmit through said substrate.

36. The connection package of claim 31, wherein said at least one external coaxial connector comprises a GPPO connector.

37. The connection package of claim 31, wherein said array of terminals comprises ball grid array ("BGA") terminals.

38. The connection package of claim 31, wherein said substrate comprises at least a first dielectric layer and a second dielectric layer.

39. The connection package of claim 31, wherein said substrate comprises a plurality of dielectric layers formed by a low-temperature co-fired ceramics process, not a printed circuit board.

40. The connection package of claim 31, wherein said substrate comprises a plurality of dielectric layers formed by a high-temperature co-fired ceramics process.

41. The connection package of claim 31, wherein said substrate is ceramic.

42. The connection package of claim 31,

wherein one of said plurality of interconnections comprises a via connection,

wherein said via connection comprises a conductor core for a signal,

wherein said conductor core is surrounded by a dielectric material portion of said substrate and bound by a circular opening for a ground signal.

43. The connection package of claim 31,

wherein said plurality of first microstrips further comprises at least a pair of co-planar ground lines;

wherein said co-planar ground lines are formed on both sides of said at least one of said plurality of first microstrips ("high-speed microstrip");

wherein both of said co-planar ground lines are for being capacitively coupled to said high-speed microstrip through a first partial length;

wherein said high-speed microstrip is widened through a second partial length to increase its capacitance.

44. The connection package of claim 31,

wherein said substrate comprises at least a first dielectric layer and a second dielectric layer,

wherein said top surface of said substrate is a top surface of said first dielectric layer,

wherein said plurality of interconnections comprise:

a plurality of second paths selectively formed between said first and second dielectric layers;

a plurality of third paths selectively formed at a bottom of said second dielectric layer,

wherein at least one of said plurality of second paths is for a ground signal and connected to at least one of said plurality of third paths through a via connection;

wherein said via connection is underneath said at least one of said plurality of first microstrips;

wherein said at least one of said plurality of second paths and said at least one of said plurality of third paths form a continuous ground path.

45. The connection package of claim 44,

wherein said at least one of said plurality of second paths is for providing substantially constant characteristic impedance along said at least one of said plurality of second paths;

wherein said via connection is for providing substantially constant characteristic impedance along said via connection;

wherein said at least one of said plurality of third paths is for providing substantially constant characteristic impedance along said at least one of said plurality of third paths.

46. The connection package of claim 44,

wherein said at least one of said plurality of first microstrips tapers out at a tapering

section,

wherein said via connection is underneath said tapering section.

47. The connection package of claim 31,

wherein said substrate comprises at least a first dielectric layer and a second dielectric layer,

wherein said top surface of said substrate is a top surface of said first dielectric layer,

wherein said plurality of interconnections comprise:

a plurality of second transmission lines selectively formed between said first and second dielectric layers;

a plurality of third transmission lines selectively formed at a bottom of said second dielectric layer,

a plurality of first via connections formed in said first dielectric layer, and

a plurality of second via connections formed in said second dielectric layer,

wherein one of said plurality of first via connections connects said at least another one of said plurality of first microstrips to one of said plurality of second transmission lines,

wherein one of said plurality of second via connections connects said one of said plurality of second transmission lines to one of said plurality of third transmission lines,

wherein said one of said plurality of first via connections is aligned with said one of said plurality of second via connections.

48. The connection package of claim 31,

wherein said at least one of said plurality of first microstrips comprises a first partial length near an inner edge of said substrate and a second partial length toward an outer edge of said substrate,

wherein a width along said second partial length is wider than a width along a portion of said first partial length.

49. The connection package of claim 48,

wherein said first partial length comprises a third partial length and a fourth partial

length,

wherein said third partial length is closer to said inner edge than said fourth partial length is to said inner edge,

wherein a width along said third partial length is wider than a width along said fourth partial length.

50. The connection package of claim 31,

wherein said substrate comprises at least a first dielectric layer, a second dielectric layer, and a third dielectric layer

wherein said top surface of said substrate is a top surface of said first dielectric layer,

wherein said plurality of interconnections comprise:

a plurality of second paths selectively formed between said first and second dielectric layers;

a plurality of third paths selectively formed between said second and third dielectric layers;

a plurality of fourth paths selectively formed at a bottom of said third dielectric layer,

wherein at least one of said plurality of second paths is for a ground signal and connected to at least one of said plurality of fourth paths through at least a first via connection and a second via connection;

wherein said at least another one of said plurality of first microstrips is connected to one of said plurality of third paths,

wherein spacing between said first via connection and said second via connection is less than a wavelength of the highest frequency signal that is to be carried along said one of said plurality of third paths.

51. The connection package of claim 50,

wherein spacing between said first via connection and said one of said plurality of third paths is about half of a separation between said at least one of said plurality of second paths and a said at least one of said plurality of fourth paths.

52. The connection package of claim 31, wherein said substrate is less than 0.4 cubic inches.

53. The connection package of claim 31,

wherein said substrate comprises at least a first dielectric layer and a second dielectric layer,

wherein said top surface of said substrate is a top surface of said first dielectric layer,

wherein said plurality of interconnections comprise:

a plurality of second paths selectively formed between said first and second dielectric layers;

a plurality of third paths selectively formed at a bottom of said second dielectric layer,

wherein at least one of said plurality of second paths is for a ground signal and connected to at least one of said plurality of third paths through a via connection;

wherein a first portion of said at least one of said plurality of first microstrips is over a portion of said at least one of said plurality of second paths,

wherein a second portion of said at least one of said plurality of first microstrips is over said via connection,

wherein a third portion of said at least one of said plurality of first microstrips is over a portion of said at least one of said plurality of third paths,

wherein said first portion is narrower than said third portion,

wherein said second portion tapers out from said first portion toward said third portion,

wherein said first portion, said second portion and said third portion are for providing substantially constant impedance along said first portion, said second portion and said third portion.

54. The connection package of claim 42,

wherein said via connection's impedance is determined by:

$$60 \log (b/a) / [\eta \times \varepsilon]$$

wherein b is a diameter of said circular opening, a is a diameter of said conductor core, ε is a dielectric constant of said dielectric material portion, and η is an efficiency of a capacitance between said circular opening and said conductor core as compared to that in a coaxial cable having same a and b dimensions.

**55.** A connection package for connecting at least one high speed integrated circuit chip ("IC"), said IC comprising at least one high speed signal and low speed signals, said connection package comprising:

(1) a substrate;

(2) means for providing external coaxial communication for said high-speed signal;

(3) means for providing external communication for at least said low speed signals, said (3) means positioned at a bottom side of said substrate;

(4) means for connecting said high speed signal between said IC and said (2) means, said (4) means selectively formed on a top surface of said substrate;

(5) means for communicating said low speed signals from or to said IC, said (5) means selectively formed on the top surface of said substrate;

(6) means for providing interconnection between said (5) means and said (3) means, said (6) means formed within said substrate;

(7) means for maintaining substantially constant characteristic impedance throughout substantially said (2) means and said (4) means;

(8) means for maintaining substantially constant characteristic impedance throughout substantially said (5) means, said (6) means, and said (3) means;

(9) means for providing less number of impedance discontinuities in said (7) means than said (8) means.

56. The connection package of claim 55,

wherein said impedance of said (7) means is better controlled than said impedance of said (8) means,

wherein said (2) means comprises external coaxial connector, said (2) means located at a

side of said substrate,

wherein said (3) means comprises BGA connectors,

wherein said (6) means comprises internal vertical coaxial connections and internal striplines.

**57.** A connection package for connecting at least one high speed integrated circuit ("IC") to a plurality of external terminals, at least one of said external terminals being a coaxial terminal, comprising:

a substrate, said substrate comprising at least a first dielectric layer and a second dielectric layer, said second dielectric layer disposed underneath said first dielectric layer;

a plurality of microstrips selectively formed on top of said first dielectric layer, said plurality of microstrips being disposed for connecting said IC to said external terminals;

at least one first ground conductor selectively formed between said first dielectric layer and said second dielectric layer;

at least one second ground conductor selectively formed at a bottom of said second dielectric layer;

at least one via connector formed in said second dielectric layer,

wherein said at least one via connector connects said at least one first ground conductor to said at least one second ground conductor,

wherein a portion of said at least one first ground conductor is underneath a first portion of one of said plurality of microstrips,

wherein said at least one via connector is underneath a second portion of said one of said plurality of microstrips,

wherein a portion of said at least one second ground conductor is underneath a third portion of said one of said plurality of microstrips,

wherein a width of said third portion is greater than a width of said first portion,

wherein said first portion is for providing a capacitance that is substantially the same as a capacitance along said third portion,

wherein a distance between said at least one first ground conductor and said one of said

plurality of microstrips is smaller than a distance between said at least one second ground conductor and said one of said plurality of microstrips.

58. The connection package of claim 57,

wherein said one of said plurality of microstrips is for conducting a signal at a rate of at least 20-Gbps adapted to connect to said coaxial terminal.

59. The connection package of claim 57,

wherein said first portion abuts said second portion,

wherein said second portion abuts said third portion.

60. The connection package of claim 57,

wherein said second portion tapers out from said first portion toward said third portion.

61. The connection package of claim 57, further comprising:

at least one pair of co-planar ground strips formed on said top of said first dielectric layer,

said at least one pair of co-planar ground strips being positioned on both sides of said one of said plurality of microstrips for connecting to said coaxial terminal,

a portion of said at least one pair of co-planar ground strips for being capacitively coupled to said one of said plurality of microstrips.

62. The connection package of claim 57, wherein said external terminals further comprise BGA connectors, said connection package further comprising:

a plurality of internal striplines formed in said substrate;

a plurality of first internal coaxial connectors formed in said substrate, said plurality of first internal coaxial connectors connecting some of said plurality of microstrips to some of said plurality of internal striplines;

a plurality of second internal coaxial connectors formed in said substrate, said plurality of second internal coaxial connectors connecting some of said plurality of internal striplines to some of said BGA connectors.

**63.** A connection package for connecting a plurality of signals of at least one

broadband high-speed integrated circuit chip ("IC") to a plurality of external terminals, comprising:

a substrate comprising a plurality of dielectric layers;

a plurality of microstrips selectively formed on top of said substrate, at least one of said plurality of microstrips ("high-speed microstrip") being disposed to conduct a high speed signal between said IC and one of said plurality of external terminals;

at least a pair of co-planar ground strips formed on top of said substrate and on both sides of said high-speed microstrip, a partial length of said pair for being capacitively coupled to a first partial length of said high-speed microstrip;

a first ground plane selectively formed at a first vertical distance below said high-speed microstrip in said substrate;

a second ground plane selectively formed at a second vertical distance below said high-speed microstrip in said substrate;

at least one via connector formed to connect said first and second ground planes;

a plurality of internal striplines selectively formed in said substrate, said plurality of internal striplines for connecting signals between said IC and a second set of external terminals;

a plurality of internal coaxial connectors selectively formed in said substrate, being adapted to connect said plurality of internal striplines through said substrate.

64. The connection package of claim 63, wherein said high-speed microstrip is widened through a second partial length while maintaining its capacitance.

65. The connection package of claim 63, wherein said at least one via connector is formed below said high-speed microstrip.

66. The connection package of claim 63, wherein said one of said plurality of external terminals connected to said high-speed microstrip is a coaxial GPPO connector.

67. The connection package of claim 63, wherein said second set of external terminals are BGA connectors.

68. The connection package of claim 63, wherein said high-speed microstrip is capable of carrying a signal at a rate of at least 30 Gbps.

69. The connection package of claim 63,

wherein at least a pair of said plurality of microstrips is formed to connect a pair of high-speed differential signals.

**70.** A connection package for connecting a plurality of signals of at least one broadband high-speed integrated circuit chip ("IC") to a plurality of external terminals, comprising:

(1) a substrate comprising a plurality of dielectric layers;

(2) means for conducting a high-speed signal between said IC and one of said plurality of external terminals;

(3) means for providing ground strips capacitively coupling to a first partial length of said (2) means;

(4) means for providing a first ground plane selectively formed at a first vertical distance below said (2) means;

(5) means for providing a second ground plane selectively formed at a second vertical distance below said (2) means;

(6) means for connecting said first and second ground planes;

(7) means for providing internal striplines selectively formed in said substrate, said means for connecting signals between said IC and a second set of external terminals;

(8) means for providing internal coaxial connectors selectively formed in said substrate, said means for connecting said internal striplines through said substrate.

**71.** A connection package for connecting a plurality of signals of at least one high-speed integrated circuit chip ("IC"), comprising:

a substrate comprising a plurality of dielectric layers;

a plurality of coaxial terminals mounted to a side of said connection package;

a plurality of BGA terminals mounted to a bottom of said connection package;

a plurality of microstrips selectively formed on a first layer of said plurality of dielectric layers, being disposed to connect to said plurality of signals,

some of said plurality of microstrips ("first microstrips") for connecting some of said plurality of signals ("first signals") to said plurality of coaxial terminals;

a plurality of internal connections selectively formed on a second layer of said plurality of dielectric layers;

a plurality of inter-layer connections selectively formed in said substrate,

said plurality of inter-layer connections connecting some of said plurality of microstrips ("second microstrips") to said plurality of internal connections and connecting said plurality of internal connections to said plurality of BGA terminals.

72. The connection package of claim 71,

wherein said plurality of microstrips comprise a pair of high speed differential signals and three co-planar ground strips, said pair of high speed differential signals for being capacitively coupled to said three co-planar ground strips through a first partial length;

wherein said pair of high speed differential signals are widened in width from an inner edge of said substrate to an outer edge of said substrate, said pair of high speed differential signals for maintaining their capacitance substantially constant.

73. The connection package of claim 71,

wherein said plurality of internal connections comprise:

internal striplines disposed to connect active signals; and

ground strips disposed to connect to ground;

wherein said plurality of inter-layer connections comprise:

internal coaxial conductors disposed to connect active signals;

via connectors disposed to connect to ground.

74. The connection package of claim 71, a path throughout substantially said first microstrips and said plurality of coaxial terminals for providing substantially constant impedance,

wherein a rate of said first signals is at least 20 Gbps.

**75.** A connection package for connecting a plurality of signals of at least one integrated circuit chip, comprising:

a substrate, said substrate comprising a first dielectric layer, a second dielectric layer, and a third dielectric layer, said second dielectric layer disposed underneath said first dielectric layer, said third dielectric layer disposed underneath said second dielectric layer,

a plurality of first microstrips on top of said first dielectric layer;

a plurality of second paths selectively formed between said first and second dielectric layers;

a plurality of third paths selectively formed between said second and third dielectric layers;

a plurality of fourth paths selectively formed at a bottom of said third dielectric layer,

wherein at least one of said plurality of second paths is for a ground signal and connected to at least one of said plurality of fourth paths through at least a first via connection and a second via connection,

said first via connection substantially disposed within said second and third dielectric layers, said second via connection substantially disposed in said second and third dielectric layers,

wherein one of said plurality of first microstrips is connected to one of said plurality of third paths,

wherein a distance between said first via connection and said second via connection is less than a wavelength of the highest frequency signal that is to be carried along said one of said plurality of third paths,

wherein a portion of said one of said plurality of third paths is located between said at least one of said plurality of second paths and said at least one of said plurality of fourth paths,

said portion of said one of said plurality of third paths for providing substantially constant characteristic impedance throughout substantially said portion of said one of said plurality of third paths.

76. The connection package of claim 75,

wherein a distance between said first via connection and said one of said plurality of third paths is about half of a separation between said at least one of said plurality of second paths and said at least one of said plurality of fourth paths.

77. The connection package of claim 75, further comprising:

a third via connection and a fourth via connection,

said third and fourth via connections connecting said at least one of said plurality of second paths to said at least one of said plurality of fourth paths,

said third via connection substantially disposed within said second and third dielectric layers,

said fourth via connection substantially disposed in said second and third dielectric layers,

wherein said first and second via connections are located along one side of said portion of said one of said plurality of third paths, along a direction of a signal flow,

wherein said third and fourth via connections are located along a second side of said portion of said one of said plurality of third path, along said direction of a signal flow,

wherein a distance between said third via connection and said fourth via connection is less than a wavelength of the highest frequency signal that is to be carried along said one of said plurality of third paths.

78. The connection package of claim 75,

wherein said distance between said first via connection and said second via connection is about a fraction of a wavelength of the highest frequency signal that is to be carried along said one of said plurality of third paths.

79. The connection package of claim 75,

wherein said highest frequency signal is at a rate of at least 1 Gbps.

80. The connection package of claim 75, further comprising:

a plurality of coaxial terminals mounted to a side of said connection package;

a plurality of BGA terminals mounted to a bottom of said connection package.

**81.** A connection package comprising:

a substrate;

a plurality of coaxial terminals located substantially at a first outer edge of said substrate;

a plurality of non-coaxial terminals located substantially at a second outer edge of said substrate;

a plurality of microstrips on said substrate;

a pair of said plurality of microstrips ("pair of microstrips") having a first length near an inner edge of said substrate and a second length near said first outer edge of said substrate, said pair of microstrips connected to said plurality of coaxial terminals;

said pair of microstrips for providing capacitive coupling to each other at said first length,

said pair of microstrips for carrying active signals,

said pair of microstrips for substantially eliminating capacitive coupling to each other at said second length,

each of said pair of microstrips having a first width at said first length, each of said pair of microstrips having a second width at said second length, said second width being greater than said first width,

said pair of microstrips for providing substantially constant characteristic impedance throughout substantially said pair of microstrips and said plurality of coaxial terminals,

some of said plurality of microstrips connected to said plurality of non-coaxial terminals;

wherein a distance between said pair of microstrips at said second length is greater than a distance between said pair of microstrips at said first length.

82. The connection package of 81, wherein said pair of microstrips is widened in width along a third length within said first length.

83. The connection package of 81, wherein a width of an inner conductor of each of

said plurality of coaxial terminals is substantially identical to a width of each of said pair of microstrips at said second length.